REMARKS

The Examiner is thanked for the due consideration given the application. The specification has been amended to improve the language.

Claims 1-7 and 9-20 are pending in the application. The amendments to claim 1 and new claims 14 and 15 find support in, e.g., Figure 1 of the application. Claim 8 has been canceled and its subject matter has been incorporated into claim 7. New claims 10 and 11 find support in, e.g., Figure 1 of the application. New claims 12 and 13 find support in, e.g., Figure 2 of the application. New claims 16-20 recite aspects of the present invention without utilizing "means plus function" terminology.

No new matter is believed to be added to the application by this amendment.

Rejection Under 35 USC §112, First Paragraph

Claims 7-9 have been rejected under 35 USC §112, first paragraph, as failing to comply with the enablement requirement. This rejection is respectfully traversed.

The Official Action asserts that "sending back switching instruction data representing port switching through the clock supply route" following a clock defect is not enabled. However, claim 8 has been incorporated into claim 7 such that this limitation now reads "sending back switching instruction

data representing port switching by coupling arbitrary virtual paths for nodes," which is clearly enabled by the disclosure.

This rejection is believed to be overcome, and withdrawal thereof is respectfully requested.

Rejections Under 35 USC §103(a)

Claims 1-5 have been rejected under USC §103(a) as being unpatentable over PUPPA et al. (U.S. Patent 7,092,361) in view of MURATA (U.S. Patent 7,177,327), and further in view of STORR (U.S. Patent 7,072,302). The teachings of PULESTON (U.S. Publication 2002/0181480) have been added to the aforesaid rejection to reject claim 6. These rejections are respectfully traversed.

The present invention pertains to an ATM system having alternative switching in case of clock failure. The present invention is illustrated, by way of example, in Figure 1 of the application, which is reproduced below.

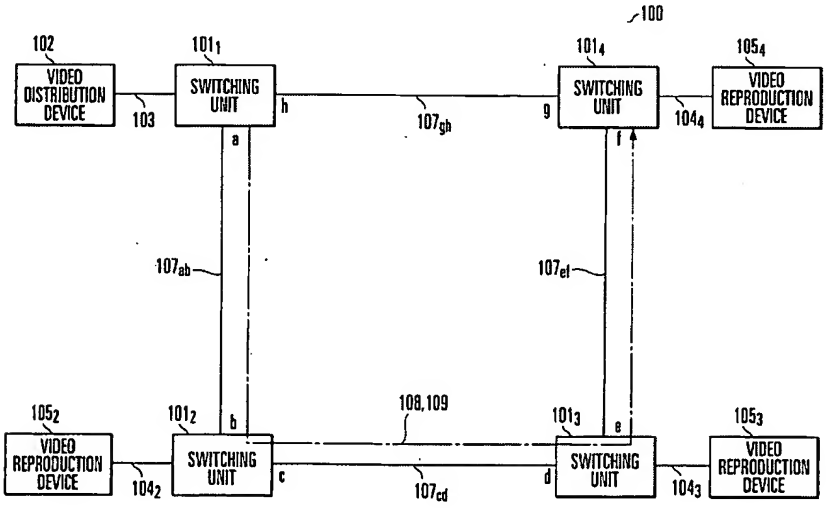


FIG. 1

Figure 1 shows a loop configuration of switching units, which allows alternative switching routes for clock signals. Claim 1 of the present invention sets forth: "at least one relay node which is positioned in a clock supply route formed by coupling arbitrary virtual paths for a loop of nodes in a network." Claim 1 of the present invention also sets forth first and second port switching means where "the first and second port switching means forming upstream and downstream switching ports."

MURATA pertains to a circuit termination apparatus. The Official Action refers to Figure 13 of MURATA, which is reproduced below.

FIG.13

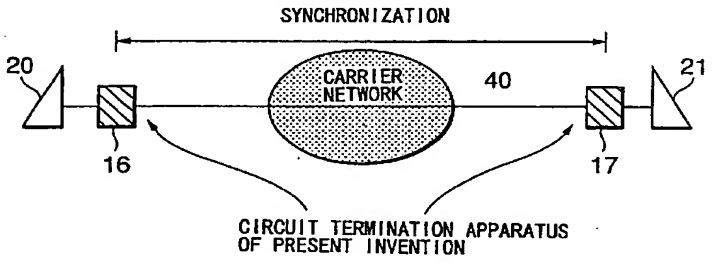


Figure 13 of MURATA shows circuit termination apparatuses 16, 17 attached linearly to a carrier network. MURATA fails to teach or suggest *inter alia* the node loop configuration of the present invention. The Official Action catalogues the failures of MURATA from page 4, line 15 to page 5, line 10.

The Official Action refers to Figures 4 and 6 of PUPPA et al. and asserts that a relay node and coupling virtual paths for a clock supply route is taught. Figure 4 of PUPPA et al. is reproduced below.

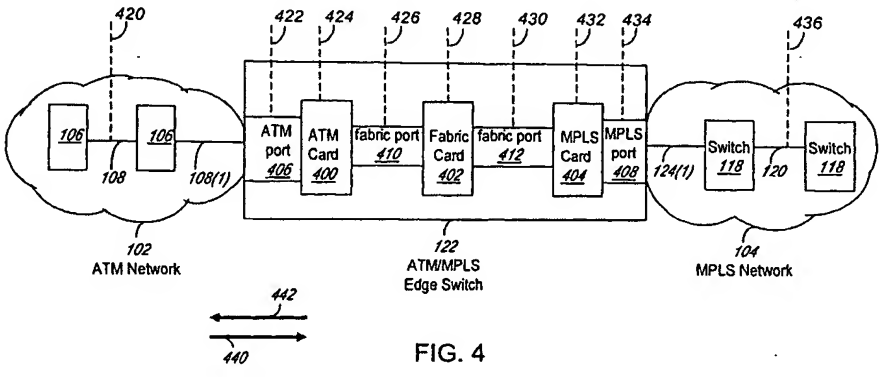


FIG. 4

Figure 4 of PUPPA et al. shows an ATM/MPLS switch connecting an ATM network to a MPLS network. However, PUPPA et al. fail to disclose a loop in which a virtual path can be formed, such as is set forth in claim 1 of the present invention.

The Official Action also refers to Figure 6 of PUPPA et al. which is reproduced below.

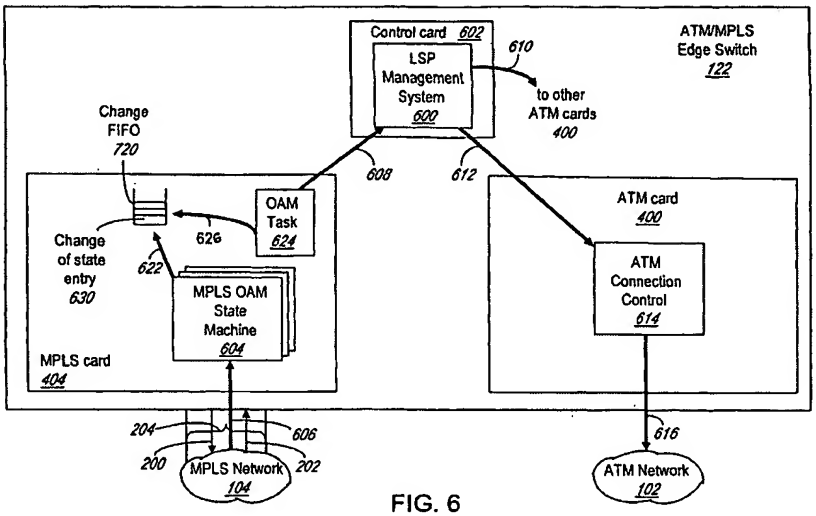


FIG. 6

Similar, Figure 6 of PUPPA et al. shows a linear switch configuration, and not a loop in which a virtual path can be formed.

Also, Figure 1 of PUPPA et al. shows four interconnected MPLS switches 118. However, these simple MPLS switches cannot perform the virtual path routing, such as is performed by the switching means of the loop of nodes of claim 1 of the present invention.

The Official Action turns to STORR for teachings pertaining to upstream and downstream side clock supply routes. However, the teachings of STORR fail to address the deficiencies of MURATA and PUPPA et al. in inferring a claimed embodiment of the present invention.

The Official Action refers to PULESTON for teachings pertaining to a priority table to reject claim 6. However, these teachings of PULESTON fail to address the deficiencies of the

other applied art in teaching or inferring base claim 1 of the present invention.

As a result, one of ordinary skill and creativity would fail to produce claim 1 of the present invention from any combination of the applied art references. A *prima facie* case of unpatentability has thus not been made. Claims depending upon claim 1 are patentable for at least the above reasons.

These rejections are believed to be overcome, and withdrawal thereof is respectfully requested.

Conclusion

The Examiner is thanked for considering the Information Disclosure Statement filed January 5, 2004 and for making an initialed PTO-1449 Form of record in the application.

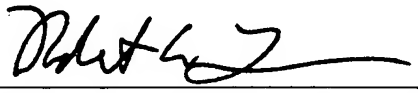
Prior art of record but not utilized is believed to be non-pertinent to the instant claims.

The Examiner's rejections are believed to have been overcome, obviated or rendered moot and that no issues remain. The Examiner is accordingly respectfully requested to place the application in condition for allowance and to issue a Notice of Allowability.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



Robert E. Goozner, Reg. No. 42,593
209 Madison Street, Suite 500
Alexandria, VA 22314
Telephone (703) 521-2297
Telefax (703) 685-0573
(703) 979-4709

REG/lrs